Pixel-level Visible Light Communication Projector with Interactive Update of Images and Data

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ABSTRACT

We previously studied methods leveraging pixel-level visible light communication (PVLC) that embeds human eye imperceptible information in each pixel of an image. In this paper, we propose a dynamic PVLC system that offers high video quality and interactively updates the PVLC information through hardware encoding processing.

1 INTRODUCTION

An augmented reality system (AR) that presents information in the real world through superimposition was studied and developed as an intuitive information media. However, most of the existing systems are limited to presenting the augmented information on a display. Display-based computing (DBC) [1] is the concept of using displays not only for presenting visual information to "humans" but also for conveying information to "physical devices," being suitable for constructing an environment in which computer graphics and physical devices could exchange information.

We previously reported on pixel-level visible light communication (PVLC) [2] that uses high-speed flickering to embed digital information in all the pixels of an image. We implemented the PVLC using a DLP projector that employs a digital micromirror device (DMD). Figure 1 shows the PVLC concept. Using the PVLC, while the visible image is presented to the users, the physical devices' photosensors can acquire the information embedded in the projected image without the need for calibration. However, the data transfer speed is low and interactive updating of the video and information cannot be realized because the conventional PVLC projector receives the encoded data from the PC using the USB 2.0 interface (i.e. all the frames are frozen in the digital domain before being transmitted to the projector).

We proposed the reconfigurable PVLC (RPVLC) framework that can interactively update the video and information by transferring data using the HDMI interface and developed the projector as its implementation suggested in [3]. However, the PC computation load and amount of data transferred between the PC and projector were excessive because both the video and data encoding processes were executed by the PC. As a result, it was impossible to achieve both high-quality images and dynamic update of the images and data.

In this paper, we propose the dynamic PVLC (DPVLC) system to address these problems. The proposed system can project a 24-bit gradation color PVLC video at 120 fps by synchronously controlling the ON/OFF states of the DMD and LED light sources at the projector's given performance limit. The proposed system can also significantly reduce the PC computation load and data transfer rate between the PC and projector by performing high-speed synchronized control of the DMD and LEDs and by encoding the PVLC images and data through hardware processing. We implemented the method using a DynaFlash projector [4] and confirmed through experiments that the performance of the proposed system matches the design parameters. Figure 2 shows the higher interactivity level achieved by the proposed system. Unlike the conventional system, that only achieves the interactivity between users and devices, the proposed system demonstrates the interactivity between users, devices, and projected images.

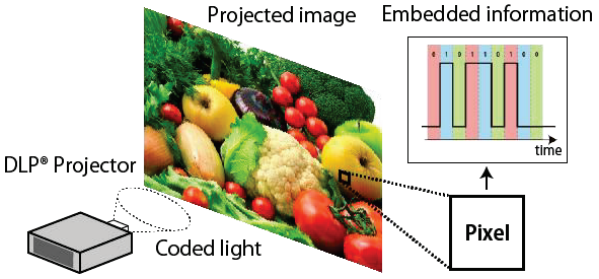

Fig. 1 The PVLC concept

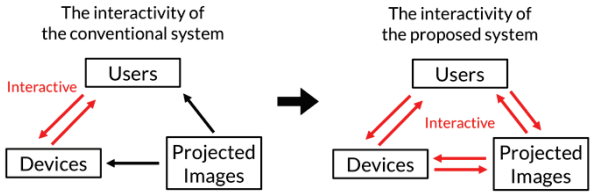

Fig. 2 Interactivity levels of the conventional system and proposed system

2 DESIGN AND IMPLEMENTATION

2.1 System Overview

In this paper, we propose a DPVLC system that can achieve both high video quality and interactive updating of the video and information, resolving the problem

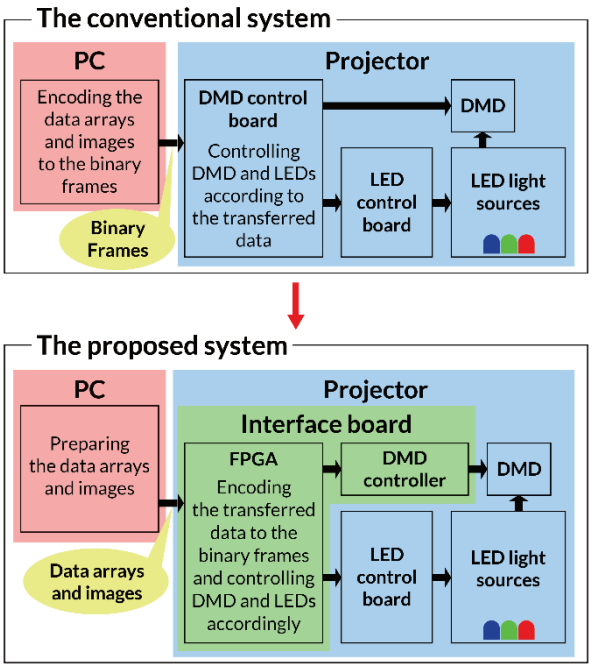

Fig. 3 Overview of the conventional versus proposed system

associated with conventional PVLC systems.

Figure 3 shows a block diagram level comparison between the conventional system (including RPVLC) and the proposed system (DPVLC).

2.2 PVLC Data Structure

The PVLC data is segmented in three parts, namely the synchronization frames, data frames, and luminance adjustment frames, that constitute altogether one frame of the PVLC video. The synchronization frames indicate the start of data, the same information being embedded in all the pixels in order to avoid a data transmission error. The data frames are composed of a pre-defined number of frames, different information being embedded in each pixel. The luminance adjustment frames correct the luminance inherently disturbed by the synchronization and data frames and compose the video perceived by a human.

2.3 Design

In the conventional system, including the RPVLC, data and images were encoded on a PC and expanded to binary images that were subsequently transferred to the projector. The associated PC computation load and the amount of transferred data were excessive. In the proposed system, images and data are transferred in their original format, while the FPGA on the projector encodes them and controls the DMD and light sources so that the PC can efficiently transfer the data to the projector.

Conversely, it is difficult to change or correct the encoding process in the proposed method since the processing flow strongly depends on the projector's hardware. Therefore, we organized and summarized the PVLC implementation and developed specifications for the

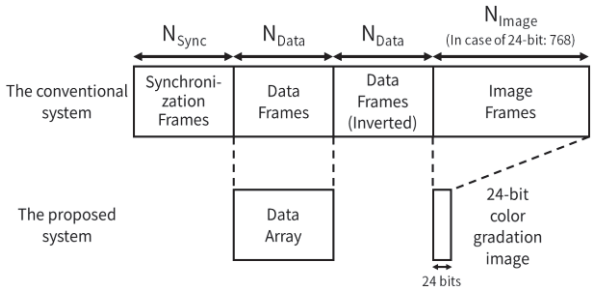

Fig. 4 Amount of transferred data in the conventional system and proposed system. N_{Sync}, N_{Data}, N_{Image} are the number of bits of the synchronization signal, transmission data, and color gradation, respectively.

PVLC data transfer protocol, demonstrating the necessary and sufficient performance requirements. We also developed the appropriate DMD and LED controls.

2.3.1 Data Transmission

Figure 4 shows a comparison of the amount of transferred data between the conventional and proposed system. In the conventional system, it was necessary to format the information to a binary data array before sending it. In the proposed system, it is possible to update the information by transmitting the data and the array of luminance values.

For example, when transferring data of 32-bit length and a 24-bit color image (excluding the synchronizing signal), the conventional system needs to transfer 832 ($32 \times 2 + 2^8 \times 3$) binary images from the PC to the projector. In the proposed system, it is sufficient to transfer only a data array of 32 bits length and a 24-bit color image (56 binary images in total).

2.3.2 DMD and LED Light Source Control

Figure 5 shows a comparison of the data structure, DMD, and LED light source control between the proposed and conventional system. In the synchronization frames, the system transmits the same blinking pattern for all the pixels. The proposed system turns on all pixels for 44 μs, which is the minimum update time of the DMD, and transmits a signal by blinking the LED light sources during the same time interval. The DMD control frequency is about 22 kHz. The synchronization frames will include the synchronization signal transmitting a maximum of 44 bits, as the minimum blinking time of the LEDs is 1 μs. The maximum blinking frequency of the LEDs is thus 1 MHz. In the data frames, both systems transmit the data signal by controlling the DMD. In the luminance adjustment frames, the system adjusts the luminance distorted by the data frames and then projects the video with 24-bit color gradation by synchronous control of the DMD and LEDs. The proposed system controls the blinking of the LEDs with a period shorter than the DMD minimum update time (44 μs) as in Watanabe et al. [4]. Thus, if the

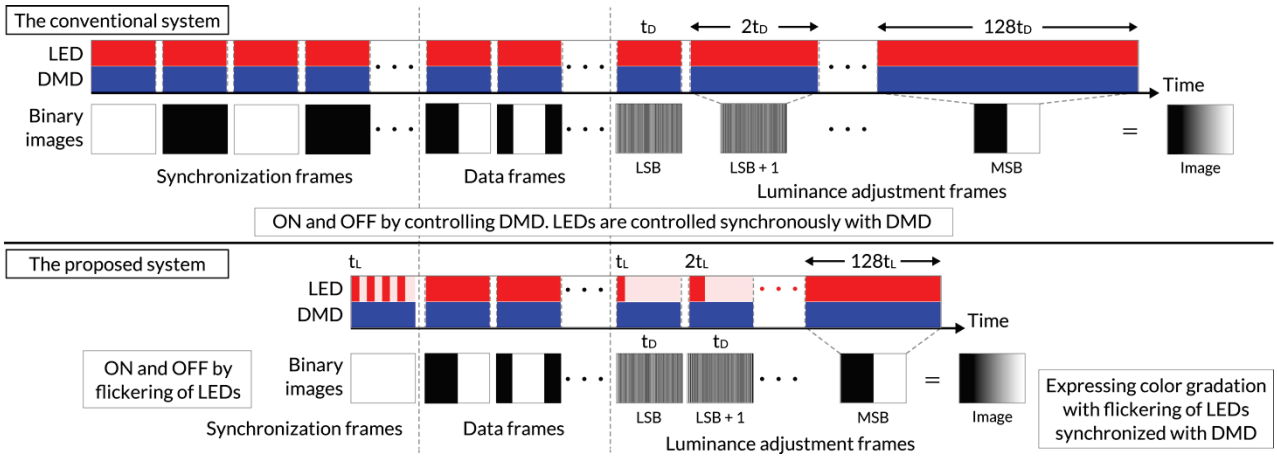

Fig. 5 Comparison of the data structure, DMD, and LED light sources control between the conventional and proposed system. t_D is the minimum update time of the DMD and t_L is the unit flickering time of the LED light sources.

projection time of the binary frames making up an image is 1080 μs or more, the proposed system can project the video with 24-bit color gradation.

2.4 Implementation

Our proposed projector has the interface board connected to the PC using the PCI Express (Gen 2 x8) bus. We implemented the DPVLC control core on an FPGA (Kintex UltraScale XCKU040-2FFVA1156E, Xilinx) residing on the interface board. The DPVLC system transmits the arrays that compose the data and images directly from the PC memory into the FPGA memory by using the Scatter-Gather Direct Memory Access (SGDMA). The system executes the PVLC encoding processing on the FPGA and generates binary images constituting the PVLC video and control information for the LED light sources. The system controls the DMD and LED light sources based on this information and projects the PVLC video.

3 EXPERIMENTS

3.1 Evaluation of Interactive Video Update

We conducted this experiment to confirm whether an interactive update of the projection video and embedded data is possible using our proposed projector.

3.1.1 Environment conditions

Our proposed projector was connected to the PC (Precision T7810, DELL), and projected the PVLC video. We developed a receiver using a photodiode (S5971, Hamamatsu Photonics) to receive the light from the projector. We placed the receiver at about 1 m from the projector and measured the output signal with an oscilloscope (TDS2024C, Tektronix). Figure 6 shows the experimental setup.

3.1.2 Settings

We implemented the program to project images for the experiments using C++ on Visual Studio 2017. We set the

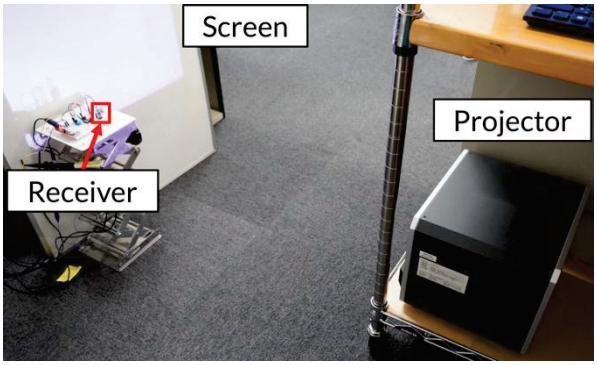

Fig. 6 Experimental setup

PVLC image frame rate of the projector to 120 Hz. The control program expanded the PVLC data and images in the PC memory as arrays that it sequentially read out and transferred to the projector. We took two measurements. First, we calculated the refresh rate of the PVLC video by measuring the interval between the projected PVLC image frames. Secondly, we measured how long it took the program to transfer the data and image arrays for 200 times and calculated the average time required for the update process.

3.1.3 Results

The time interval between the PVLC image frames was 8.36 ms, from which the refresh rate for the PVLC video was computed as 119.6 Hz. This result closely matches the value set as the refresh rate (120 Hz), so the proposed projector satisfies the designed performance. The average time intervals required to transfer the data and image arrays were 1.68 ms and 0.76 ms, respectively, while in the worst case it took 3 ms and 1 ms, respectively. Even in the worst case, these times summed up to 4 ms, that is shorter than the image projection period of 8.33 ms at the 120 Hz refresh rate. It was thus shown that the design performance for the transfer time was also satisfied.

3.2 Evaluation of Data Transmission

We conducted this experiment to confirm whether the PVLC signals efficient transmission is possible by using high-speed blinking of the LED light sources synchronously with the ON/OFF states of the DMD.

3.2.1 Environment conditions

We performed this experiment under the same conditions as in Section 3.1.1. Hereby, the receiver is required to decode 1 MHz high-speed blinking light, thus the receiver was designed accordingly.

3.2.2 Settings

Our proposed system projected the PVLC video using the same program as in Section 3.1.2. We set the PVLC image frame rate to 120 Hz as in Section 3.1.2. We configured the PVLC data structure as one frame for the synchronization and 64 frames for the data, assigning the remaining 120 binary frames as the luminance adjustment frames. We transmitted the synchronizing signal by flickering the LED light sources at 1 MHz (the maximum value in the design) while the synchronization and data signals were set as pulsed waveforms. Therefore, the synchronization frames include the synchronizing signal of 44 bits because the pulse width of the synchronization signal is 1 μs and the number of the synchronization frames is 44 We used a 1 μs square wave as the synchronization signal and a 44 μs pulsed wave in all pixels as data signal. We measured the synchronization and data signal waveforms while the projected light was received by using the receiver and the oscilloscope.

3.2.3 Results

Figure 7 shows the synchronization signal as a 1 μs periodic waveform. Figure 8 shows the waveform of the synchronization and data signals. The synchronization signal is periodically turned on and off at high speed in synchronicity with the ON/OFF states of the DMD. The same data signal can also be used as a pulsed waveform by the ON/OFF states of the DMD. Therefore, the proposed system can efficiently transmit a signal by

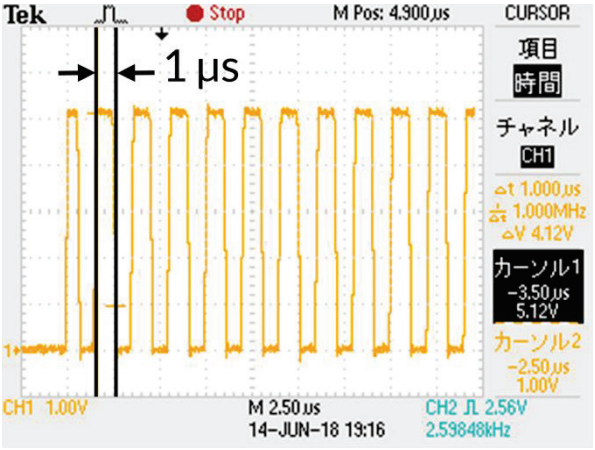

Fig. 7 The synchronization signal

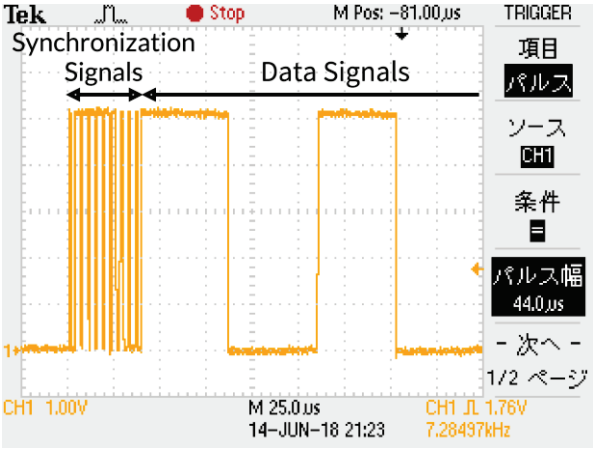

Fig. 8 The synchronization and data signal

combining the synchronization signal transmission through the blinking LED light source and data signal transmission implemented in the DMD ON/OFF states.

4 CONCLUSION

In this paper, we proposed a new PVLC system to achieve the dynamic updating of video and information. The proposed system can project a 24-bit color gradation PVLC video at a refresh rate of 120 Hz by the synchronous control of the ON/OFF states of a DMD and the fast blinking of an LED light source. Moreover, we demonstrated a method to drastically reduce the PC computation load and amount of transferred data by executing a high-speed synchronized control of the DMD and LEDs and by encoding the PVLC video in the hardware. We experimentally confirmed that the proposed system could achieve the target design performance.

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REFERENCES

[1] M. Sugimoto, K. Kodama, A. Nakamura, M. Kojima, and M. Inami, “A Display-Based Tracking System: Display-Based Computing for Measurement Systems,” Proc. ICAT, pp. 31–38, 2007.

[2] S. Kimura, R. Oguchi, H. Tanida, Y. Kakehi, K. Takahashi, and T. Naemura, “PVLC Projector: Image Projection with Imperceptible Pixel-Level Metadata,” ACM SIGGRAPH 2008 Posters on, Article No.135, 2008.

[3] L. Zhou, S. Fukushima, and T. Naemura, “Dynamically Reconfigurable Framework for Pixel-level Visible Light Communication Projector,” Proc. SPIE 8979, 89790J–14, 2014.

[4] Y. Watanabe, G. Narita, S. Tatsuno, T. Yuasa, K. Sumino, M. Ishikawa, “High-speed 8-bit Image Projector at 1,000 fps with 3 ms Delay,” Proc. IDW, pp.1064-1065, 2015.